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| EXAMINER | |
|---|---|
| VIGUSHIN, JOHN B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2827 | |

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/033,990 | SHAH ET AL. | |
| | Examiner | Art Unit | |
| | John B. Vigushin | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *11-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0502*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-10 and 18-24, drawn to a circuit board apparatus with interposer and a processor package structure, classified in class 361/767 and class 324/765, respectively.

II. Claims 11-17, drawn to a circuit board apparatus with interposer structure and gasket, classified in class 361, subclass 719.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case: The combination (Invention II) as claimed does not require the particulars of the subcombination (Invention I) as claimed because claims to both the subcombination and combination are presented and assumed to be patentable, and the omission of details of the claimed subcombination in the combination claim is evidence that the patentability of the combination does not rely on the details of the specific subcombination. The subcombination (Invention I) has separate utility such as a circuit board apparatus not requiring a gasket.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

6. During a telephone conversation with Jonathan M. Harris on April 1, 2004, a provisional election was made with traverse to prosecute the invention of Claims 1-10 (Invention I) because the restriction as presented to Mr. Harris by the Examiner originally had three Inventive groups (Group I: Claims 1-10; Group II: Claims 11-17; Group III: Claims 18-24). The Examiner has reconsidered the restriction requirement and now considers Claims 18-24 as proper for examination along with Claims 1-10. Therefore, the Examiner has added Claims 18-24 to Applicant's elected Group I. Accordingly, Claims 1-10 and 18-24 will receive a first action on the merits, below. Affirmation of this election must be made by Applicant in replying to this Office action. Claims 11-17 are withdrawn from further consideration by the Examiner, according to 37 CFR 1.142(b), as being drawn to a non-elected invention.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

### *Claim Rejections - 35 USC § 112*

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said PCB " in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitation "the interposer" in line 4. There is insufficient antecedent basis for this limitation in the claim: Is the recited interposer structure that of **only one** of the two interposers, or, **each** of the two interposers? The claim needs to be amended accordingly.

Claim 4 recites the limitation "the interposer." There is insufficient antecedent basis for this limitation in the claim: Is the recited interposer structure that of **only one** of the two interposers, or, **each** of the two interposers? The claim needs to be amended accordingly.

Claim 7 recites the limitation "the interposer" in line 2. There is insufficient antecedent basis for this limitation in the claim: Is the recited interposer structure that of **only one** of the two interposers, or, **each** of the two interposers? The claim needs to be amended accordingly.

Claim 8 recites the limitation "the interposer" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim: Is the recited interposer structure that of **only one** of the two interposers, or, **each** of the two interposers? The claim needs to be amended accordingly.

Claim 9 recites the limitation "the semiconductor contact pads" in line 1. There is insufficient antecedent basis for this limitation in the claim: There is no *semiconductor* antecedent; only a "semiconductor package," or, a "substrate," as recited in base Claim 1. Therefore, the rejection may be overcome by inserting --package-- after "semiconductor" in line 1 of Claim 9, or, replacing "semiconductor" with --substrate-- in line 1 of the Claim 9.

Claims 2, 3, 5, 6 and 10 depend from rejected base Claim 1 and therefore inherit the defects of the claim.

## Rejections Based On Prior Art

10. The following references were relied upon for the rejections hereinbelow:

Pasco et al. (US 6,319,829 B1) Love (US 5,477,160)

Barrett (US 6,081,429) Morris et al. (US 6,020,749)

Alagaratnam et al. (US 6,335,491 B1)

***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-4 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Pasco et al.

As to Claim 1 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection set forth above), Pasco et al. discloses, in Fig. 4: a semiconductor package 40 defined by a substrate 44 having a matrix of conductive contact pads on both the top and bottom surfaces of substrate 44; two interposers 48 for receiving semiconductor package 40 (col.4: 11-17), each of the two interposers 48 defined by a body 20 having a matrix of interposer contact bumps 38 on both the inner and outer surfaces of body 20, each interposer contact bump 38 comprising an electrically conductive path and shaped to abut a contact pad 34P of semiconductor package 40 (compare Figs. 3 and 4) and contact pads of PCB 50 (the PCB contact pads are shown in Fig. 4 but not labeled with a reference number).

As to Claim 2, Pasco et al. further discloses the contact pads 34P of the semiconductor package (corresponding to each of the two interposers 48) are uniformly spaced.

As to Claim 3, Pasco et al. further discloses semiconductor package 44 is a land grid array package composed of lands 34P (Figs. 3 and 4; col.4: 11-14).

As to Claim 4 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection set forth above), Pasco et al. further discloses contact pads 30 of each of the two interposers 48 are uniformly spaced (Fig. 4).

As to Claim 8 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection set forth above), Pasco et al. further discloses the interposer pads 30 on the inner surface of each of the two interposers 48 are arranged in the same pattern, pitch and spacing as the contact pads 34P on the "top" surface of semiconductor package 40, wherein "top" and "bottom" surfaces are relative terms, not limited to their representation in the Drawings: i.e., the surface of semiconductor package 40 having pads 34P can just as well be the "top" surface relative to an electronic system reference point of an observer; e.g., if the assembly of Fig. 4 is turned "upside down" in an electronic system application relative to an observer, then the pads 34P are on the "top" surface of semiconductor package 40.

13. Claims 18-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Love.

As to Claim 18, Love discloses, in Fig. 14: a processor 1310 comprising substrate 1311 having a matrix of conductive contact pads on the bottom surface of the

substrate 1311 and a test port (for connection of test chip processor 1312 thereto) on the top surface of substrate 1311 (col.14: 32-37and 51-56).

As to Claim 19, Love further discloses, in Fig. 14, the test port comprises a conductive contact pad (for connection of processor chip 1312 thereto; col.14: 32-35).

As to Claim 20, Love further discloses the test port is designated for debugging and test operations (col.9: 5-9; col.14: 33-45).

As to Claim 21, Love further discloses the contact pads on the bottom surface of the processor 1310 are designated for production operations; i.e., testing an unknown multichip module for production operations (increasing production yield; col.14: 46-50; col.15: 20-24).

As to Claim 22, Love further discloses the test port on the top surface of substrate 1311 possesses approximately the same contact density as the contact pads on the bottom surface of substrate 1311 (Fig. 14).

### *Claim Rejections - 35 USC § 103*

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

15. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pasco et al. in view of Barrett and Morris et al.

A) As to Claim 5:

I. Pasco et al. discloses contact pads on the top surface of semiconductor package 40 that correspond to and receive the solder bumps 46 for electromechanically joining semiconductor chips 42 to semiconductor package 40. Pasco et al. does not teach that the top surface contact pads support debugging and test operations.

II. Barrett discloses a semiconductor package comprising semiconductor die 30, interposer substrate 10 and carrier 40 wherein the contact pads 22 on the top surface of the semiconductor package (which is the top surface of interposer substrate 10) support test operations by test apparatus 50 (Fig. 3A; col.4: 19-40; col.7: 31-33 and 43-51)

III. Morris et al. also discloses a semiconductor package comprising semiconductor elements 101, 103 and teaches that each of the interposer substrates 105, 106 of the semiconductor package can support both debugging and test operations (Figs. 1B, 2 and 4; col.2: 60-col.3: 6; col.3: 64-col.4: 1).

IV. Since Pasco et al. discloses contact pads on the top surface of the semiconductor package 40, and since Pasco et al., Barrett and Morris et al. are all in

the semiconductor package fabrication and application arts, then the use of the accessible top surface of the semiconductor package of Barrett for testing, and furthermore, for testing AND debugging, as taught by Morris et al., by way of contact pads on the accessible surface of the semiconductor package, as taught by Barrett, would have been readily recognized for use in the accessible portions of the top surface of the semiconductor package in the pertinent art of Pasco et al. for ensuring the proper functioning and overall operational reliability of the semiconductor package.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide, among the contact pads in the accessible top surface of substrate 44 of the semiconductor of Pasco et al., test contact pads for connection to a test apparatus, as taught by Barrett, for performing test operations and, as further taught in the similar semiconductor package of Morris et al., for also performing debugging, in order to ensure the proper functioning and overall operational reliability of the semiconductor package in Pasco et al., as taught by Barrett and Morris et al.

B) As to Claim 6, modified Pasco et al. further discloses that contact pads 34P on the bottom surface of the semiconductor package 40 are designated for production operations; i.e., soldering to interposers 48 (Figs. 3 and 4; col.4: 11-14).

17. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pasco et al., as applied to Claim 8 above, and further in view of Alagaratnam et al.

As to Claim 9 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection set forth above):

I. Pasco et al. discloses contact pads 34P on the bottom surface of semiconductor package 40 (Figs. 3 and 4) but is silent as to the pitch of the contact pads.

II. Alagaratnam et al. discloses that the semiconductor contact pads (corresponding to and receiving bumps 212) of package 204 have a 1.27 mm pitch which is taught as a standard that is old and well-known in the art (Figs. 1A and 2; col.1: 35-38; col.7: 44-55).

III. Since both Pasco et al. and Alagaratnam et al. are both in the semiconductor packaging art, the use of the industry standard contact pad pitch on the semiconductor package, as taught by Alagaratnam et al. would have been readily recognized in the pertinent art of Pasco et al. for standard electronic applications.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the semiconductor package contact pads at the standard pitch of 1.27 mm in order to form a semiconductor package assembly for use in standard electronic applications, as taught by Alagaratnam et al.

18. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pasco et al.

I. Pasco et al. discloses all the limitations of the base claim including a semiconductor package substrate 44 with contact pads on the top and bottom surfaces for establishing connections to chips 42 and interposers 48, respectively (Fig. 4), but does not teach that substrate 44 supports 1443 signals to be collected.

II. However, it would have been an obvious matter of design choice to modify the circuit and contact pad layout of the semiconductor package substrate in Pasco et al. such that it supports exactly 1443 signals to be collected by the semiconductor package, since the Applicant has not disclosed that supporting exactly 1443 signals to be collected by the semiconductor package substrate solves any stated problem, produces any unexpected result, or is for any particular purpose, and it appears that the substrate of the invention would function equally well supporting any number of signals required to be collected by the substrate for an electronics application. .

19. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Love.

As to Claims 23 and 24:

Love is silent as to the whether the test port on the top surface of substrate 1311 possesses approximately the same signal integrity as the contact pads on the bottom surface of substrate 1311; also, Love is silent as to the whether the test port on the top surface of substrate 1311 possesses approximately the same reliability as the contact pads on the bottom surface of substrate 1311. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the contact pads at the test port (top surface) and on the bottom surface of substrate 11, and design the supporting circuitry of substrate 11 such that both test port and bottom surface contact pads exhibited the same signal integrity and operational reliability in order to ensure that the testing and debugging operations for the multichip modules under test

repeatedly produce accurate results and thereby increase the production yield of the semiconductor devices being made, as disclosed by Love (col.1: 32-34; col.15: 21-24).

### *Allowable Subject Matter*

20. Claim 7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

21. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 7, patentability resides in the limitation wherein *the number of interposer contacts on the inner surface of the interposer exceeds the number of contact pads on the top the surface of the semiconductor package*, in combination with the other limitations of the claim.

22. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

### *Conclusion*

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Spielberger et al. (US 6,657,134 B2) discloses an LGA package 10 mounted on an interposer 30 having solder bumps on each side for connecting LGA package 10 to circuit board 25 (Figs. 1, 4 and 5).

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Primary Examiner
Art Unit 2827

jbv
April 4, 2004